1.4.2 The Fetch-Execute Cycle

May/June 2003. P3

4. The next instruction to be carried out is

LDAN 25

which loads the number 25 into the accumulator.

With reference to the special registers in a processor, describe the stages of the fetch-execute cycle when dealing with this instruction. **[6]**

Oct/NOV 2003

5. Describe the fetch/decode/execute/reset cycle when an ADD instruction is being executed.

You should include

- Program Counter (PC)

-Memory Address Register (MAR)

-Memory Data Register (MDR)

-Current Instruction Register (CIR)

-Accumulator

in your answer. **[7]**

Oct/NOV 2004

5 (a) Describe the stages of the fetch/decode/execute/reset cycle, explaining how the special registers in the processor are used. You should use as an example the processing of a jump instruction. **[9]**

May/June 2005

2. JUMP 300 is an instruction to be executed by a processor. It means that the next instruction the processor should process is held in location 300. Describe the stages of the fetch/decode/execute cycle and the effects on the contents of the registers in the processing of this instruction. **[7]**

Oct/NOV 2005

4. A processor is to carry out the instruction ADD 200. This instruction means that the contents of memory location 200 should be added to the accumulator.

Describe the steps of the fetch-execute cycle, stating the effect on the registers in the processor, when carrying out this instruction. **[8]**

1.4.2 The Fetch-Execute Cycle

Oct/NOV 2007

9. (b) Describe two stages of the fetch/execute cycle which would change the contents of the MAR. State clearly, in each case, what the MAR contains. **[4]**

May/June 2008

6. (a) (i) State what is held in the Program Counter (PC) during the fetch/execute cycle. **[1]**

(ii) Explain how the contents of the PC change during the fetch/execute cycle. **[4]**

(b) Describe the contents of the memory address register (MAR) during the fetch/execute cycle. **[4]**

May/June 2009

5. (b) At a particular point in a program, the program counter (PC) contains the value 200.

(i) State the expected value contained in the PC after the instruction held at location 200 has been fetched.

Explain your answer. **[2]**

Oct/NOV 2009. P33

5. Describe the fetch/decode/execute/reset cycle when a jump instruction is being processed. **[6]**

May/June 2010. P31/ P32

8. State what is stored in each of the following special purpose registers in a computer and explain how the contents are altered during the fetch/execute cycle.

(i) MAR **[3]**

(ii) MDR (or MBR) **[3]**

(iii) CIR **[3]**

May/June 2010. P33

8. State what is stored in each of the following special purpose registers in a computer and explain how the contents are altered during the fetch/execute cycle.

(i) PC (or SCR) **[3]**

(ii) CIR **[3]**

(iii) IR (Index Register) **[3]**

1.4.2 The Fetch-Execute Cycle

Oct/NOV 2010. P31

3. (b) (i) Explain what the accumulator holds and how the contents change during the fetch-execute cycle. **[2]**

(ii) Explain what the program counter (PC) holds and how the contents change during the fetch-execute cycle. **[3]**

May/June 2011. P32

11. (b) When a program is run the processor uses special purpose registers.

Describe how the contents of each of the following registers changes during the fetch-execute cycle:

(i) Memory Address Register (MAR) **[2]**

(ii) Memory Data Register (MDR) **[2]**

May/June 2011. P33

11. (b) When a program is run the processor uses special purpose registers. One of these registers is the Program Counter (PC).

Describe how the content of the PC changes during the fetch-execute cycle. **[4]**

Oct/NOV 2011. P31

2(b) Describe the use of the following special purpose registers and how they change during the fetch-execute cycle.

(i) Program Counter (PC) **[3]**

(ii) Current Instruction Register (CIR) **[3]**

Oct/NOV 2011. P32

2 (a) Describe the use of the following special purpose registers and how they change during the fetch-execute cycle.

(i) Memory Address Register (MAR) **[3]**

(ii) Index Register (IR) **[3]**

Oct/NOV 2011. P33

2 (a) Describe the use of the Memory Data Register (MDR).

Explain how the contents change during the fetch-execute cycle. **[3]**

Oct/NOV 2012. P31

3 Most modern computers are designed using Von Neumann architecture.

1.4.2 The Fetch-Execute Cycle

(a) Describe what is meant by Von Neumann architecture. **[2]**

(b) The sequence of operations below shows the fetch stage of the fetch-execute cycle in register transfer notation.

1. MAR ← [PC]

2. PC ← [PC] + 1

3. MDR ← [[MAR]]

4. CIR ← [MDR]

Note:

• [register] denotes the contents of the specified register

• Step 1 above is read as 'The contents of the Program Counter are copied to the Memory Address Register'.

(i) Explain what is happening at step 2. **[1]**

(ii) Explain what is happening at step 3. **[1]**

(iii) Describe the two remaining steps needed to complete the fetch-execute cycle. **[2]**

Oct/NOV 2012. P32

3 (a) The sequence of operations below show - in register transfer notation - the fetch stage of the fetch-execute cycle.

1. MAR ← [PC]

2. PC ← [PC] + 1

3. MDR ← [[MAR]]

4. CIR ← [MDR]

Note: [register] denotes the contents of the specified register

Step 1 above is read as 'The contents of the Program Counter are copied to the Memory Address Register'.

(i) Describe what is happening at step 4. **[1]**

(ii) Explain how the data bus is used at step 3. **[1]**

(iii) Explain how the address bus is used at step 3. **[1]**

1.4.2 The Fetch-Execute Cycle

Oct/NOV 2012. P33

3 (a) The sequence of operations below shows the fetch stage of the fetch-execute cycle in register transfer notation.

1. MAR ← [PC]

2. PC ← [PC] + 1

3. MDR ← [[MAR]]

2150

4. CIR ← [MDR]

Note:

• [register] denotes the contents of the specified register

• Step 1 above is read as 'The contents of the Program Counter are copied to the Memory Address Register'.

(i) Explain what is happening at step 4. **[1]**

(ii) Explain what is happening at step 3. **[1]**

Oct/NOV 2013.P32

Q3)(c) The diagram shows a program loaded into main memory starting at memory address 30 Hex.

Main memory (contents shown in Hex.)

Address	
30	2150
31	A351
32	A552
33	FFFF
58	003C
59	103C
5A	010B

(ii) Describe the steps in the fetch stage of the fetch-execute cycle. Refer to the instruction at address 30 to illustrate your answer. **[5]**

1.4.2 The Fetch-Execute Cycle

A351
A552
FFFF

003C
103C
010B

Oct/NOV 2014.P31

5 Most modern computers are designed using Von Neumann architecture.

(b) The sequence of operations below shows the fetch stage of the fetch-execute cycle in register transfer notation.

1. MAR ← [PC]

2. PC ← [PC] + 1

3. MDR ← [[MAR]]

4. CIR ← [MDR]

Note: [register] denotes the contents of the specified register.

Explain what is happening at the fetch stage. **[4]**

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8(c) The table shows six stages in the von Neumann fetch-execute cycle. Put the stages into the correct sequence by writing the numbers 1 to 6 in the right hand column.

Description of stage	Sequence number
the instruction is copied from the Memory Data Register (MDR) and placed in the Current Instruction Register (CIR)	
the instruction is executed	
the instruction is decoded	
the address contained in the Program Counter (PC) is copied to the Memory Address Register (MAR)	
the value in the Program Counter (PC) is incremented so that it points to the next instruction to be fetched	

the instruction is copied from the memory location contained in the Memory Address Register (MAR) and is placed in the Memory Data Register (MDR)	

[6]

May/June 2015.P13

5(b) The sequence of operations shows, in register transfer notation, the fetch stage of the fetchexecute cycle.

1 MAR ← [PC]

2 PC ← [PC] + 1

3 MDR ← [[MAR]]

4 CIR ← [MDR]

• [register] denotes contents of the specified register or memory location

• step 1 above is read as "the contents of the Program Counter are copied to the Memory Address Register"

(i) Describe what is happening at step 2. **[1]**

(ii) Describe what is happening at step 3. **[1]**

(iii) Describe what is happening at step 4. **[1]**

(d)(ii) Explain the actions of the processor when an interrupt is detected. **[4]**

May/ June 2016. P11/ P12

3 (a) Describe how special purpose registers are used in the fetch stage of the fetch-execute cycle. **[4]**
(b) Use the statements A, B, C and D to complete the description of how the fetch-execute cycle handles an interrupt.

A	the address of the Interrupt Service Routine (ISR) is loaded to the Program Counter (PC).
B	the processor checks if there is an interrupt.
C	when the ISR completes, the processor restores the register contents.
D	the register contents are saved.

At the end of the cycle for the current instruction ..... .
If the interrupt flag is set, ... , ... and ..... .
The interrupted program continues its execution. **[4]**