1.4.1 CPU Architecture

May/June 2004

3. (a) Describe what is meant by Von Neumann architecture. **[3]**

(b) Explain the purpose of each of the following special registers in a processor.

(i) Program Counter (Sequence Control Register). **[2]**
(ii) Current Instruction Register. **[2]**
(iii) Memory Address Register. **[2]**
(iv) Memory Data Register. **[2]**
(v) Accumulator. **[2]**

Oct/NOV 2006

1 (a) Describe the purpose of the following registers in a processor:

(i) Current instruction register (CIR), **[2]**
(ii) Memory address register (MAR), **[2]**
(iii) Program counter (PC), **[2]**
(iv) Index register (IR). **[2]**
(v) Current instruction register (CIR), **[2]**

May/June 2007

7. (a) Describe what is meant by Von Neumann architecture. **[2]**

Oct/NOV 2007

9. (a) State the purpose of the Memory Address Register (MAR) in a computer. **[1]**

May/June 2008

6. (a) (i) State what is held in the Program Counter (PC) during the fetch/execute cycle. **[1]**

(ii) Explain how the contents of the PC change during the fetch/execute cycle. **[4]**

(b) Describe the contents of the memory address register (MAR) during the fetch/execute cycle. **[4]**

Oct/NOV 2008

8. (a) Describe basic Von Neumann architecture of a computer. **[3]**

May/June 2009

5. (a) Describe basic Von Neumann processor architecture. **[3]**

1.4.1 CPU Architecture

Oct/NOV 2010. P31/ P32

3. (a) Explain what is meant by Von Neumann architecture. **[3]**

May/June 2011. P31/ P32

1 Name three different types of bus in a processor and state what each is used for. **[6]**

Oct/NOV 2011. P31

2 (a) Explain what is meant by Von Neumann architecture. **[3]**

(b) Describe the use of the following special purpose registers and how they change during the fetch-execute cycle.

(i) Program Counter (PC) **[3]**
(ii) Current Instruction Register (CIR) **[3]**

Oct/NOV 2011. P32

2 (a) Describe the use of the following special purpose registers and how they change during the fetch-execute cycle.

(i) Memory Address Register (MAR) **[3]**
(ii) Index Register (IR) **[3]**

(b) Explain how the address bus and the data bus are used in a computer. **[3]**

Oct/NOV 2011. P33

2 (a) Describe the use of the Memory Data Register (MDR).

Explain how the contents change during the fetch-execute cycle. **[3]**

(b) Name three types of bus that are used in a computer. For each one explain what it is used for. **[6]**

Oct/Nov 2013. P31

3 (a) Most modern computers are designed using Von Neumann architecture. Explain what is meant by Von Neumann architecture. **[2]**

Oct/Nov 2013. P32

3 (a) Describe what is meant by a register.

[2]

1.4.1 CPU Architecture

Computer Science (9608)

May/ June 2015. P11/ P12

8 (a) Explain how the width of the data bus and system clock speed affect the performance of a computer system.

Width of the data bus

Clock speed

[3]

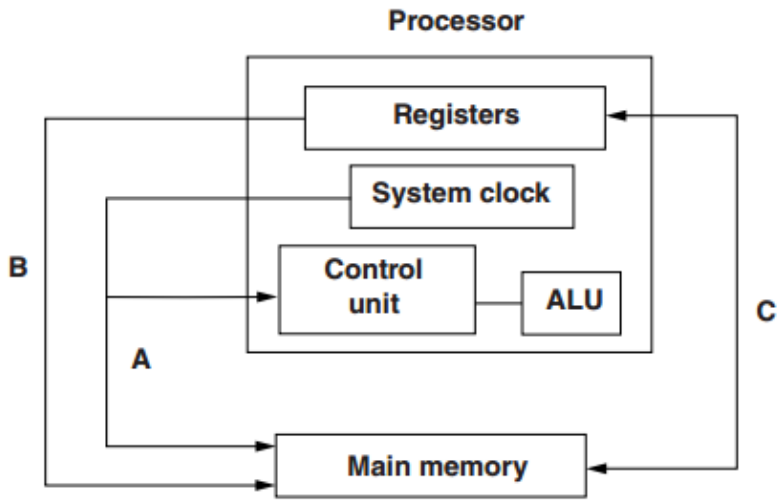
(b) Most computers use Universal Serial Bus (USB) ports to allow the attachment of devices. Describe two benefits of using USB ports. **[2]**

May/ June 2015. P13

5 (a) Name and describe three buses used in the von Neumann model. **[6]**

Oct/Nov 2015. P11/P13

2 (a)



The diagram above shows a simplified form of processor architecture.
Name the three buses labelled A, B and C. **[3]**

(b) State the role of each of the following special purpose registers used in a typical processor.

Program Counter
Memory Data Register
Current Instruction Register
Memory Address Register **[4]**

1.4.1 CPU Architecture

Oct/Nov 2015. P12

6 (a) Describe the stored program concept for the basic Von Neumann model for a computer system. **[3]**

(b) (i) Name the three types of bus used by a processor. **[3]**

(ii) State the function of the system clock in a processor. **[1]**

May/June 2018. P11

8 The Von Neumann model uses a series of registers.
(a) Explain what is meant by the term **register**. **[2]**
(b) (i) Explain the purpose of the Memory Data Register (MDR). **[2]**
(ii) Name **two** registers, other than the MDR, that are used in the fetch-execute cycle. **[2]**