3.3.5 RISC Processors

4 (a) Three descriptions and two types of processor are shown below.
Draw a line to connect each description to the appropriate type of processor.

Description	Type of processor
Makes extensive use of general purpose registers	RISC
Many addressing modes are available	CISC
Has a simplified set of instructions	

[3]

(b) In a RISC processor three instructions (A followed by B, followed by C) are processed using pipelining.
The following table shows the five stages that occur when instructions are fetched and executed.

(i) The 'A' in the table indicates that instruction A has been fetched in time interval 1.
Complete the table to show the time interval in which each stage of each instruction (A, B, C) is carried out.

Stage	Time interval								
	1	2	3	4	5	6	7	8	9
Fetch instruction	A								
Decode instruction									
Execute instruction									
Access operand in memory									
Write result to register									

[3]

(ii) The completed table shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.
Calculate how many clock cycles are saved by the use of pipelining in the above example.
Show your working. **[3]**